In the Claims:

Claims 2-4 and 38-40 are canceled. All pending claims and their present status are produced below.

1. (Canceled)

2.-4. (Canceled)

5. (Previously Presented) A deserializer for receiving data transmitted over a network, the deserializer in a universal serializer/deserializer programmable for implementing two or more communications protocols, the deserializer comprising:

a programmable receive data circuit for receiving the data, for performing initial data receive functions, and for coupling to a network connection;

a synchronization circuit for selectably detecting a synchronization pattern in the data, the synchronization circuit configured to be programmed with the synchronization pattern corresponding to a current protocol of the two or more communications protocols, and coupled to the programmable receive data circuit for signaling a match signal in response to matching the synchronization pattern with the data;

a selectable CRC circuit for detecting errors in the data and determining integrity of the data, the selectable CRC circuit coupled to the programmable receive data circuit for signaling in response to detecting an error in the data;

a data storage device for storing the data to be accessed by a CPU, the data storage device coupled to the programmable receive data circuit for receiving the data; and

an interrupt generator for generating interrupt signals in response to interrupt generating signals, the interrupt generator coupled to the programmable receive data circuit, the selectable CRC circuit, the synchronization circuit, and the data storage device for receiving the interrupt generating signals, and coupled to the CPU for providing the interrupt signals.

6. (Previously Presented) The deserializer of claim 5, wherein the protocol specific receive functions comprise at least one of decoding the data according to a decoding scheme, separating clock signals from data signals in the data, inverting polarity of the data signals, and storing the data into a shift register.

7. (Previously Presented) The deserializer of claim 6, wherein the decoding scheme is one of Manchester decoding scheme or Non-Return-to-Zero Inverted ("NRZI") decoding scheme.

8. (Previously Presented) The deserializer of claim 5, wherein the programmable receive data circuit further comprises hardware that enables a receive function required for at least two of the two or more communications protocols.

9. (Previously Presented) The deserializer of claim 5, wherein the synchronization circuit is not selected in response the current protocol being a UART protocol.

10. (Previously Presented) The deserializer of claim 5, wherein the synchronization pattern programmed in the synchronization circuit is a logic 00000001 and the current protocol is USB 1.1.

11. (Previously Presented) The deserializer of claim 5, wherein the selectable CRC circuit is a module implementing a CRC function from software instructions.

12. (Previously Presented) The deserializer of claim 5, further comprising an END-OF-PACKET detector for selectably detecting an End-Of-Packet pattern, the End-Of-Packet detector configured to be programmed with the End-Of-Packet pattern corresponding to the current protocol of the two or more communications protocols, configured to not operate in response to not being selected, and configurable to couple to the network connection for receiving the data and to the interrupt generator for signaling an End-Of-Packet detection.

13. (Previously Presented) The deserializer of claim 12, wherein the End-Of-Packet pattern programmed in the End-Of-Packet detector is one of a two single ended zeros and a J-state according to a USB 1.1 protocol and a high pulse held in a range of 62.5 to 600 nanoseconds according to a 10-base T protocol.

14. (Previously Presented) The deserializer of claim 12, wherein the End-Of-Packet detector further comprises:

a register for storing the End-Of-Packet pattern programmed in the End-Of-Packet detector; and

a comparator coupled to the programmable receive data circuit and the register for comparing the data with the End-Of-Packet pattern.

15. (Previously Presented) The deserializer of claim 5, wherein the data storage device is one of a programmable data storage unit and a non-programmable double buffer.

16. (Previously Presented) The deserializer of claim 15, wherein the data storage device is the programmable data storage unit configured to be programmed to modify its data storage capability to meet the requirements of the protocol.

17. (Previously Presented) The deserializer of claim 5, wherein the data storage device further comprises a set of selectable buffers, the data storage device configured to receive a program signal indicating a bit limit for the current protocol of the two or more communications protocols and coupled to the interrupt generator for providing a signal in response to reaching the bit limit.

18. (Previously Presented) The deserializer of claim 17, wherein the data storage device is further configured to select a number of buffers of the set of selectable buffers, the number of buffers corresponding to a number of data bits required to store a bit limit number of bits.

19. (Previously Presented) A data receive circuit for a deserializer in a universal programmable serializer/deserializer having a synchronization circuit, a data storage device and a CRC circuit for implementing a programmed protocol from a set of communications protocols, the data receive circuit comprising:

an exclusive-OR gate (XOR) configurable to be coupled to a network connection for receiving an input signal carrying a data and for selectably performing a polarity inversion of the input signal;

a polarity inverter coupled to the XOR for inverting the input signal and configured to receive a first program signal indicating whether the programmed protocol requires the polarity inversion;

a clock detection and configuration circuit coupled to the XOR for detecting a protocol specific start condition of the programmed protocol selected from a set of programmed start condition patterns and for providing a protocol specific clock signal of the programmed protocol selected from a set of programmed clock signal definitions in response to receiving a protocol selection indicating the programmed protocol;

a clock/data separation circuit coupled to the clock detection and configuration circuit for selectably providing separation of clock information from data information in the input signal in response to receiving the protocol selection indicating the programmed protocol;

a decoder coupled to the clock/data separation circuit for selectably performing a protocol specific decoding function of the programmed protocol selected from a set of programmed decoding functions in response to receiving the protocol selection indicating the programmed protocol;

a multiplexer coupled to the clock detection and configuration circuit, to the clock/data separation circuit, and to the decoder for supplying the protocol selection and configured to receive a second program signal indicating the requirements of the programmed protocol;

a receive shift register coupled to the decoder, to the synchronization circuit, to the CRC circuit and to the data storage device, the receive shift register for receiving the data one bit at a time from the decoder and providing the data, several bits at a time, to the synchronization circuit, the CRC circuit, and the data storage device;

a control logic circuit coupled to the receive shift register, and the synchronization circuit, the control logic for receiving a synchronization match signal from the synchronization circuit and for instructing the receive shift register to provide the data to one of the synchronization device and the data storage device and for setting a number of bits in the several bits used in accordance to the programmed protocol in response to a third program signal indicating the number of bits required by the programmed protocol.

20. (Previously Presented) The data receive circuit of claim 19, wherein the first program signal is a bit of a protocol selection word.

21. (Previously Presented) The data receive circuit of claim 19, wherein the set of programmed start condition patterns programmed in the clock detection and configuration circuit comprises an Inter-Integrated-Circuits ("I^2C") falling edge with a high clock, a UART falling edge, a SPI rising clock edge.

22. (Previously Presented) The data receive circuit of claim 19, wherein the clock detection and configuration circuit further comprises:

a clock sampler having an edge detector coupled to the XOR for sampling the clock to detect the rising and falling edges of the input signal in detecting the protocol specific start condition of the programmed protocol; and

a phase lock loop for generating a clock signal with a programmable frequency and a programmable phase in providing the protocol specific clock signal of the programmed protocol;

23. (Previously Presented) The data receive circuit of claim 19, wherein the multiplexer bypasses one or more of the clock detection and configuration circuit, the clock/data separation circuit, and the decoder in response to the second program signal indicating the programmed protocol requirements.

24. (Previously Presented) The data receive circuit of claim 19, wherein the clock/data separation circuit further selectably provides clock division of the clock signal as required by the programmed protocol.

25. (Previously Presented) The data receive circuit of claim 19, wherein the set of programmed decoding functions of the decoder comprises a function from the group consisting of a Non-Return-to-Zero Inverted ("NRZI") decoding function and a Manchester decoding function.

26. (Previously Presented) The data receive circuit of claim 25, wherein the function from the group consisting of a Non-Return-to-Zero Inverted ("NRZI") decoding function and a Manchester decoding function of the decoder are programmed in a hardware implementation for being performed faster than decoding functions programmed in a software implementation.

27. (Previously Presented) The data receive circuit of claim 19, wherein the decoder further selectably performs bit unstuffing in response to being required by the programmed protocol.

28. (Previously Presented) The data receive circuit of claim 19, wherein the control logic circuit is further coupled to a shift count register indicating a number of bits loaded into the receive shift register.

29. (Previously Presented) The data receive circuit of claim 28, wherein the number of bits loaded into the receive shift register is used in response to the programmed protocol not having a fix number of bits.

30. (Previously Presented) A synchronization circuit for a deserializer in a universal programmable serializer/deserializer having a data receive circuit, the serializer/deserializer for implementing a programmed protocol from a set of communications protocols, the synchronization circuit comprising:

a synchronization register configured to receive a first program signal indicating a synchronization pattern corresponding to the programmed protocol;

a programmable synchronization mask coupled to the synchronization register through as set of logic gates for masking out a corrupted bit for optimizing the synchronization circuit to operate in a particular environment, the programmable synchronization mask configured to receive a program signal indicating settings for the masking; and

a comparator coupled to the programmable receive data circuit for receiving an input data signal and coupled to the logic gates for receiving the synchronization pattern, the comparator for comparing the synchronization pattern with the input data signal and for producing a match signal in response to matching the synchronization pattern with the input data signal.

31. (Previously Presented) The data receive circuit of claim 30, wherein the logic gates are AND gates which modify the corrupted bit by changing a logic value of the corrupted bit to a programmed logic value indicated by the settings.

32. (Previously Presented) The data receive circuit of claim 30, wherein the comparator is a digital comparator.

33. (Previously Presented) A serializer for transmitting data over a network, the serializer in a universal serializer/deserializer programmable for implementing two or more communications protocols, the serializer comprising:

a data buffer for receiving the data to be transmitted from a processor and configured to receive a load signal for loading off the data;

a transmit shift register coupled to the data buffer for loading the data off the data buffer, the shift register further for serially shifting the data out;

a control logic circuit coupled to the data buffer for providing the load signal and configured to receive a bit number corresponding the a current protocol of the two or more communications protocols, wherein the load signal is provided upon reaching a bit-number number of bits received by the data buffer; and

a programmable encoder coupled to the transmit shift register for receiving the shifted out data, for selectably performing an encoding function required for the current protocol in response to receiving a protocol selection signal indicating the current protocol, and for transmitting the data out of the serializer.

34. (Previously Presented) The serializer of claim 33, wherein the control logic circuit further comprises a shift counter configured to receive a program signal indicating the bit

number and configured to count a number of bits received by the data buffer and to indicate the number of bit reaching the bit-number.

35. (Previously Presented) The serializer of claim 33, further comprising an End-Of-Packet generator coupled to the control logic circuit and to the programmable encoder for selectably generating a End-Of-Packet pattern corresponding to the current protocol in response to receiving a last bit signal from the control logic circuit and for providing the End-Of-Packet pattern to the programmable encoder for transmission.

36. (Previously Presented) The serializer of claim 33, further comprising a programmable idle circuit for selectably providing an idle signal corresponding to the current protocol in response to the transmit shift register having no data to transmit.

37. (Previously Presented) The serializer of claim 36, wherein the idle signal is one of an all logic zero state, an all logic one state, and a tri-state.

38.-40. (Canceled)